IN THE CLAIMS:

1-27. (Canceled).

28. (Currently Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT,

wherein an active layer of the n-channel TFT is sandwiched by a first wiring line and a second wiring line through insulating layers,

wherein the active layer includes a low concentration impurity region that is in contact with a channel formation region; ~~and~~

wherein the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line; and

wherein the first wiring line is electrically connected with the second wiring line.

29. (Canceled).

30. (Previously Presented) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT,

wherein an active layer of the n-channel TFT is sandwiched by a first wiring line and a second wiring line through insulating layers; and

wherein the second wiring line has a portion being a laminate of a first conductive layer and a second conductive layer, and a portion being a laminate of the first conductive layer, the second conductive layer and a third conductive layer.

31. (Previously Presented) The semiconductor device according to claim 30, wherein the third conductive layer has a lower resistance value than the first conductive layer and the second conductive layer.

32. (Previously Presented) The semiconductor device according to claim 30, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

33. (Previously Presented) The semiconductor device according to claim 30, wherein the third conductive layer mainly contains one of aluminum (Al) and copper (Cu).

34. (Currently Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed by an n-channel TFT,

wherein the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers,

wherein the active layer includes a low concentration impurity region that is in contact with a channel formation region; ~~and~~

wherein the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line; and

wherein the second wiring lines has a portion being a laminate of a first conductive layer and a second conductive layer, and a portion being a laminate of the first conductive layer, the second conductive layer and a third conductive layer.

35. (Previously Presented) The semiconductor device according to claim 34, wherein the first wiring line is kept at one of a ground electric potential and a source power supply electric potential.

36. (Previously Presented) The semiconductor device according to claim 34, wherein the first wiring line is kept at a floating electric potential.

37. (Previously Presented) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed by an n-channel TFT,

wherein the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers, and

wherein the second wiring line has a portion being a laminate of a first conductive layer and a second conductive layer, and a portion being a laminate of the first conductive layer, the second conductive layer and a third conductive layer.

38. (Previously Presented) The semiconductor device according to claim 37, wherein the third conductive layer has a lower resistance value than the first conductive layer and the second conductive layer.

39. (Previously Presented) The semiconductor device according to claim 37, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

40. (Previously Presented) The semiconductor device according to claim 37, wherein the third conductive layer mainly contains one of aluminum (Al) and copper (Cu).

41. (Previously Presented) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on a same substrate,

wherein each of a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit has a structure including an active layer sandwiched by each of a first wiring line and a second wiring line through insulating layers;

wherein each of the active layers includes a low concentration impurity region that is in contact with each of channel formation regions;

wherein each of the low concentration impurity regions is formed to overlap each of the first wiring lines and not to overlap each of the second wiring lines;

wherein at least one of the second wiring lines has a portion being a laminate of a first conductive layer and a second conductive layer, and a portion being a laminate of the first conductive layer, the second conductive layer and a third conductive layer; and

wherein the first wiring line of the pixel TFT is kept at one of a fixed electric potential and a floating electric potential, and the first wiring line of the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line of the n-channel TFT included in the driver circuit.

42-44. (Canceled)

45. (Previously Presented) The semiconductor device according to claim 41, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

46. (Canceled).

47. (Previously Presented) The semiconductor device according to any one of claims 28 to 41 and 45, wherein the semiconductor device is one of an active matrix liquid crystal display and an active matrix EL display.

48. (Previously Presented) The semiconductor device according to any one of claims 28 to 41 and 45, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, and a portable information terminal.

49-54. (Canceled).

55. (Currently Amended) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on a same substrate,

wherein each of a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit has a structure including an active layer sandwiched by each of a first wiring line and a second wiring line through insulating layers;

wherein each of the active layers includes a low concentration impurity region that is in contact with each of channel formation regions;

wherein each of the low concentration impurity regions is formed to overlap each of the first wiring lines and not to overlap each of the second wiring lines; and

~~wherein the first wiring line of the pixel TFT is kept at one of a fixed electric potential and a floating electric potential, and the first wiring line of the n-channel TFT included in the~~

~~driver circuit is kept at the same level of electric potential as the second wiring line of the n-channel TFT included in the driver circuit~~

wherein the first wiring line in the driver circuit is electrically connected with the second wiring line in the driver circuit.

56. (Currently Amended) The semiconductor device according to claim 55, wherein the semiconductor device is one of an active matrix liquid crystal display and an active matrix EL display.

57. (Currently Amended) The semiconductor device according to claim 55, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, and a portable information terminal.

58. (Previously Presented) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on a same substrate,

wherein each of a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit has a structure including an active layer sandwiched by each of a first wiring line and a second wiring line through insulating layers;

wherein at least one of the second wiring lines has a portion being a laminate of a first conductive layer and a second conductive layer, and a portion being a laminate of the first conductive layer, the second conductive layer and a third conductive layer, and

wherein the first wiring line of the pixel TFT is kept at one of a fixed electric potential and a floating electric potential, and the first wiring line of the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line of the n-channel TFT included in the driver circuit.

59. (Previously Presented) The semiconductor device according to claim 58, wherein the third conductive layer has a lower resistance value than the first conductive layer and the second conductive layer.

60. (Previously Presented) The semiconductor device according to claim 58, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

61. (Previously Presented) The semiconductor device according to claim 58, wherein the third conductive layer mainly contains one of aluminum (Al) and copper (Cu).

62. (Currently Amended) The semiconductor device according to claim 58, wherein the semiconductor device is one of an active matrix liquid crystal display and an active matrix EL display.

63. (Currently Amended) The semiconductor device according to claim 58, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, and a portable information terminal.

64. (Previously Presented) The semiconductor device according to claim 28, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

65. (Previously Presented) The semiconductor device according to claim 30, wherein the first wiring line is electrically connected with the second wiring line.

66. (Previously Presented) The semiconductor device according to claim 34, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

67. (Previously Presented) The semiconductor device according to claim 37, wherein the first wiring line is kept at one of a ground electric potential and a source power supply electric potential.

68. (Previously Presented) The semiconductor device according to claim 37, wherein the first wiring line is kept at a floating electric potential.

69. (Previously Presented) The semiconductor device according to claim 41, wherein the first wiring line of the n-channel TFT is electrically connected with the second wiring line of the n-channel TFT.

70. (Previously Presented) The semiconductor device according to claim 41, wherein the third conductive layer has a lower resistance value than the first conductive layer and the second conductive layer.

71. (Previously Presented) The semiconductor device according to claim 41, wherein the third conductive layer mainly contains one of aluminum (Al) and copper (Cu).

72. (Canceled).

73. (Previously Presented) The semiconductor device according to claim 55, wherein at least one of the each of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

74. (Previously Presented) The semiconductor device according to claim 58, wherein the first wiring line of the n-channel TFT is electrically connected with the second wiring line of the n-channel TFT.